REMARKS

Claims 1, 3-14 and 16-24 are currently active.

Antecedent support for the amendment to the claims regarding the plurality of fabrics is found in figure 3.

The Examiner has rejected Claims 1, 3, 4, 14, 16 and 17 as being unpatentable over Sindhu in view of Manning. Applicants respectfully traverse this rejection.

Referring to Sindhu, there is disclosed a high-speed switching device. Sindhu teaches in a packet switching system, a source 10 is connected to one or more routers 20 for transmitting packets to one or more destinations 30. Each router 20 includes an input switch 100, and output switch 102, a memory 104 including one or more memory banks 105, a controller 106 and a plurality of input and output ports 107 and 108, respectively. Associated with the controller 106 is controller memory 109 for storing a routing table. Packets are received at input port 107, transferred to input switch 100 and stored temporarily in memory 104. When the packet is received by switch 100, a key is read from the first data block in the packet and transferred to controller 106. The key contains destination information which is derived from the header fields associated with the first block of data in a packet. A route

lookup engine 110 and controller 106 performs a search based on the key information and returns a result which includes the output port associated with the destination. Output switch 102 transfers the notification to the identified output port 108. Upon receiving notification information, the output port 108 initiates the transfer of the packet from memory 104 through output switch 102 back to the appropriate input port 108. Each input port 107 includes a line input interface 300, a data handler 304 and a cell output port 306. Packets are received at line input interface 300. As the packets are received, data handler 302 divides the packets received into fixed length cells. As the data handler divides the incoming packet into fixed link cells, it synchronously outputs the cells to input switch 100 through cell output port 306. See column 4, lines 14-61.

Sindhu teaches a single cell is transferred from input port 107 to input switch 100 at each cell slot. The data format for each cell transferred from an input port to input switch 100 includes an internal header and a cell data field. The input switch 100 includes a round robin data handler 500, one or more input port interfaces, one or more memory interfaces, a like plurality of pointers, and output processor 505, one or more port interfaces, and a reservation table 508, an indirect cell processor, controller interface and read controller 516. Round robin data handler 500 receives cells for each input port and transfers them to output processor 505 for output to an appropriate memory bank 105 in memory 104. See column 5, lines 19-41.

Round robin data handler 500 and output processor 505 transfers cells out to memory 104 on transmission lines 460. Round robin data handler 500 time division multiplexes the transfers to output processor 505 such that consecutive cells from the same input port are written to consecutive memory banks 105 in memory 104. Round robin data handler 500 includes a key reading engine 514 for determining the key information associated with a first cell in a packet and a linking engine 515 for linking cells in the same packet. Linking engine 515 determines the starting address in memory for the first cell to a given packet. See column 6, lines 1-34.

As is apparent from the above description, there is no teaching or suggestion of the limitation of sending portions of the packet as stripes to each fabric, let alone there being a plurality of fabrics, as found at applicants' claimed invention.

Referring to Manning, there is disclosed a redundant switch system and method of operation. The system and method are directed to eliminating or reducing the disadvantages that occur in a redundant system when a transition occurs from a system or circuit operating in the foreground to a system or circuit operating in the background. Often, when a circuit or module fails, the backup circuit is not properly initialized or operating correctly resulting in data loss or a complete system failure. See column 1, lines 40-55.

Manning teaches a control and a data interconnection between a first module 14 and a foreground switch control module 10 of a digital communications switch. Also present are a plurality of additional modules 16 and 18. Each of the plurality of modules are interconnected with foreground switch control modules 10 in the same manner that the first module 14 couples to foreground switch control module 10. A background switch control module 12 is also provided with interconnects to each of the plurality of modules in the same manner that foreground switch control module 10 interconnects to each of these plurality of modules. Background switch control module 12 operates in the background and serves as a redundant module in the event that foreground switch control module 10 fails or is taken out of service. See column 2, lines 49-65.

In operation, Manning teaches the plurality of modules receive information from a corresponding communications link using a variety of access technologies. Each module provides this information to the inputs of a foreground switch fabric 26 of foreground switch control module 10 and background switch control module 12. Foreground switch control module 10, using a foreground switch fabric controller 24 and any available switching scheme, controls the switching of foreground switch fabric 26 so that the communications information provided to each module is properly routed or mapped to the appropriate destination module. Foreground switch control module 10 receives control information from

the various modules to assist with carrying out the switching scheme. First module 14 is representative of the plurality of modules. See column 2, line 65-column 3, line 14.

The foreground switch control module 10 and background switch control module 12 are essentially interchangeable modules with one operating in the foreground and the other operating in the background to provide a redundant system to increase overall system availability. See column 4, lines 23-30.

As is clear from the above description, Manning does teach a plurality of switches, with a very specific context. The context is that each module corresponds with only a single switch control module foreground and a switch control module background. The data from any given module only goes to a corresponding foreground switch control module and background switch control module. Furthermore, it is the same data from any given module that is duplicated and goes to both the foreground switch control module and the background switch control module. Thus, Manning does not teach the limitation of "the striper sending portions of the packet as stripes to each fabric," but only to a corresponding foreground and background switch control modules. Manning also does not teach or suggest the limitation that "the transferring mechanism transfers return portions of the packet as fixed length segments as the fixed line segments are received," as found in Claim 1. In fact, Manning is totally silent regarding this limitation. Manning could care less about such a limitation.

Again, what Manning is concerned about is avoiding inefficiency when transitioning from the foreground switch to the background switch.

The Examiner is combining Sindhu and Manning to arrive at Claim 1 of applicants. However, it is respectfully submitted there must be some teaching or suggestion within the references themselves to combine the teachings the Examiner is relying upon to arrive at applicants' invention of Claim 1.

It is respectfully submitted the Examiner is using hindsight to arrive at applicants' claimed invention. Hindsight is not patent law. The Examiner is using the limitations of Claim 1 as a road map to find the various limitations in the disparate references, and having supposedly found these different limitations and the different references, concludes that applicants' claimed invention is arrived at.

Furthermore, the Examiner cannot take the teachings from these references out of the context in which they are found. Applicants do not suggest that they discovered the use of a plurality of switches. Applicants do take the position that their use of a plurality of fabrics in conjunction with the striper and the transfer mechanism and the other limitations of Claim 1 are novel and unique. By following the law, taking the teachings in the context in which they are found, the teachings of the references of the applied art cannot be combined.

The context of Manning is in regard to an input/output module that sends the data it receives only to the corresponding foreground and background switch control modules so that if the foreground switch control module fails for any reason, the background switch control module can take over without loss of data. The background switch control module basically does not do anything unless the foreground switch control module fails. In contrast, Sindhu teaches the data from the input ports are all directed to input switch 100 which then sends the data on to the memory 104. These contexts are very distinct and cannot be combined.

The question must also be raised why would one skilled in the art attempt to modify the architecture taught by Sindhu with the architecture taught by Manning since there is absolutely no need, teaching or suggestion of the input switch 100 being changed into a plurality of switches, with a foreground switch control module and a background switch control module being aligned with each input port. This is in direct conflict with the very teachings of Sindhu which requires all input ports to be connected to the single input switch 100. It will require significant research and development to take the teachings of Manning in the context in which they are found and apply them to the teachings of Sindhu to make an operational system. This only further supports applicants' position that Claim 1 is not obvious from the applied art of record. Accordingly, Claim 1 is patentable over the applied art of record.

Claims 3 and 4 are dependent to parent Claim 1 and are patentable for the reasons Claim 1 is patentable.

Claim 14 is patentable for the reasons Claim 1 is patentable.

Claims 16 and 17 are dependent to parent Claim 14 and are patentable for the reasons Claim 14 is patentable.

The Examiner has rejected Claims 5-8 and 18-20 as being unpatentable over Sindhu. Applicants respectfully traverse this rejection. Claims 5-8 and 18-20 are dependent to parent Claims 1 and 14, respectively, and are patentable for the reasons Claims 1 and 14 are patentable.

The Examiner has rejected Claims 9-13 and 21-24 as being unpatentable over Sindhu in view of Manning and further in view of Peterson. Applicants respectfully traverse this rejection.

In regard to Petersen, Petersen teaches a sublayer 301 called the segmentation and reassembly sublayer. The segmentation and reassembly sublayer is invoked if a user data packet is so long that segmentation is necessary to avoid sending user data to a receiving entity

and a minicell whose length, excluding the header, exceeds a predefined maximum length. See column 3, lines 23-32.

Petersen teaches a sending entity 401, an interconnecting link 402, and a receiving entity did 403. The sending entity contains the segmentation part of the segmentation and reassembly sublayer and a receiving entity contains the reassembly part of the segmentation and reassembly sublayer. The interconnection link carries the ATM cells from the sending entity to the receiving entity, and the ATM cells, in turn, carry the segment of the user data in minicells. See column 3, lines 33-44. Unlike the known ATM protocol model, there is no longer a 1-to-1 correspondence between each user data packet in each mini cell. Moreover, a single minicell can overlap no more than one ATM cell border as compared to the known protocol model. This is because the length of each mini cell, is limited to a length that is less than the ATM cell payload. See column 3, lines 45-56.

As is apparent from the above description of Peterson, there is no teaching or suggestion of the limitation of sending portions of the packet as stripes to each fabric, let alone there being a plurality of fabrics, as found at applicants' claimed invention. Claims 5-8 and 18-20 are patentable over the applied art of record.

In view of the foregoing amendments and remarks, it is respectfully requested that the outstanding rejections and objections to this application be reconsidered and withdrawn, and Claims 1, 3-14 and 16-24, now in this application be allowed.

Respectfully submitted,

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